REMARKS

The claims are claims 1, 3 to 5, 9 to 11 and 13 to 17.

Claims 3 and 4 are amended. Claims 2, 6 to 8 and 12 are canceled. Claim 3 is amended to depend upon claim 1 rather than canceled claim 2. Claim 4 is amended to change the recitation of the exponentiation to the superscript form. New claims 16 and 17 are added. These claims recite the sign extension on shifting disclosed in the application at page 18, lines 22 to 26.

Claims 1, 3 to 5, 10, 11, 13 and 14 were rejected under 35 U.S.C. 102(e) as anticipated by Baudendistel U.S. Patent No. 6,209,012.

Claims 1 and 13 recite subject matter not anticipated by Baudendistel. Claim 1 recites "rounding the combined product to form an intermediate result; and shifting the intermediate result a selected amount to form a final result." Claim 13 recites "an arithmetic circuit connected to receive a plurality of products from the plurality of multipliers" and "a shifter connected to receive an output of the arithmetic circuit." The OFFICE ACTION cites bit manipulation unit 22 and column 5, lines 5 to 10 as anticipating this subject matter. The Applicant respectfully submits that the above quoted portion of claims 1 and 13 require a different order of operation than taught in Baudendistel. This portion of claim 1 recites rounding to form an intermediate result, the shifting the intermediate result. This recitation clearly requires the rounding to occur before the shifting. Claim 13 recites the shifter as receiving the output of the arithmetic circuit. This also clearly requires that the rounding be accomplished in the arithmetic circuit before the shifting in the shifter. Baudendistel teaches the opposite order of operations. Baudendistel teaches adder 58 of Figure 4 performs the rounding operation. Baudendistel states at column 5, lines 13 to 17:

"The embodiment of FIG. 4 is realized in the DAU, D, of FIG. 1. The shift operation is performed by the BMU 22. The shifted out bit is stored temporarily in a register such as the PSW056. This bit is used in a subsequent adder operation performed by the adder circuit 58 in the ALU 24."

Temporary storage of the shifted out bit for a subsequent adder operation for the rounding requires the shift to precede the rounding. Figure 4 of Baudendistel illustrates in Figure 4 the shifted data word 50 from bit manipulation unit 22 supplies one input of adder 58 of arithmetic logic unit 24. This order of operations is contrary to the clear requirement of claims 1 and 13. Accordingly, claims 1 and 13 are allowable over Baudendistel.

Claims 3 and 14 recite subject matter not anticipated by Baudendistel. Claim 3 recites "the step of rounding adds a rounding value to the combined product via an arithmetic circuit having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value." Claim 14 recites "the arithmetic circuit has a carry input connected to a mid-position, wherein the carry input is asserted in response to the rounding dot product instruction." Baudendistel states at column 4, line 67 to column 5, line 4:

"An S&R bit 46 defined, for example, in the auc0 register 26 (FIG. 1) specifies whether the most significant bit ("MSB") 48 of the bits shifted out of a data word 50 is routed to the carry input of bit 0 (52) of the subsequent adder."

The subsequent adder is adder 58 illustrated in Figure 4. This disclosure clearly states that the rounding bit is supplied to the carry input of bit 0, the least significant bit of adder 58. This is not the same as the "carry input to a mid-position" recited in claim 3 nor the "carry input connected to a mid-position" recited

in claim 14. Accordingly, claims 3 and 14 are not anticipated by Baudendistel.

Claim 4 recites subject matter not anticipated by Baudendistel. Claim 4 recites "the rounding value is 2^n and the selected shift amount is n+1." The OFFICE ACTION cites column 4, line 50 of Baudendistel as anticipating this subject matter. Baudendistel states at column 4, line 50:

"a0 = a0 + p0 + p1 >> 15"

This portion of Baudendistel clearly teaches a shift value of 15. According to the limitations of claim 4 the rounding value must be 2^{14}. Note that if n + 1 is n, then n is 14. Baudendistel teaches at column 5, lines 13 to 17 a single rounding bit input to adder 58. This cannot be the rounding value of 2^{14} required by claim 4. Accordingly, claim 4 is allowable over Baudendistel.

Claim 5 recites subject matter not anticipated by Baudendistel. Claim 5 recites that n is fixed at fifteen. According to base claim 4, if the value of n is fifteen, then the rounding value is 2^{15} and the shift amount is (n + 1) 16. Contrary to requirement of claim 5, column 4, line 50 of Baudendistel discloses a shift of 15. Accordingly, claim 5 is allowable over Baudendistel.

Claim 9 was rejected under 35 U.S.C. 103(a) as made obvious by Baudendistel U.S. Patent No. 6,209,012. The OFFICE ACTION states at paragraph 7:

> "Re claim 9, Baudendistel further discloses in Figures 1 and 4 further disclose the step of forming treats both of the first and second pair of elements as signed number values (col. 3 lines 2-4). However, the examiner takes an official notice that the unsigned multiplication is less complex than the signed multiplication. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the second pair of

elements as unsigned number for unsigned multiplication in Baudendistel's invention because it would enable to reduce the circuitry and improve the system performance in general."

Claim 9 recites subject matter not made obvious by Baudendistel. Claim 9 recites "the step of forming treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value." The Examiner is correct that unsigned multiplication is less complex than signed multiplication and that replacing both inputs to one multiplier with unsigned numbers is obvious. However, the recitations of claim 9 require that one input of one product is signed and the other is unsigned. The Applicant respectfully submits that this mixed signed/unsigned input is not obvious from Baudendistel. Accordingly, claim 9 is allowable over Baudendistel.

New claims 16 and 17 recite subject matter not anticipated by or made obvious by any of the cited references. These claims require sign extension upon a right shift operation. None of the references teach such sign extension. Accordingly, claims 16 and 17 are allowable.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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